13.3 A 1.2V 121-Mode CT ΔΣ Modulator for Wireless Receivers in 90nm CMOS

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The increasing number of wireless-connectivity and cellular products drives the need for flexible receiver systems that are able to operate optimally in different modes. However, the individual blocks in the receive path have specific design requirements and multi-mode capability can only be achieved with significant flexibility of the analog blocks and in particular of the ADC.

In the past, several semi-flexible multi-mode ADCs were presented [1, 2], that cope with at most 3 modes. In this paper, a CT ΔΣ modulator is described, that is programmable over 2 decades of signal bandwidth, covering the bandwidth requirements of GSM to WLAN/WiMaX applications. The corresponding DR varies from 85 to 52dB and the clock frequency is programmable from 13 to 400MHz. An FOM between 0.2 and 0.8pJ/conversion is achieved depending on the mode.

Figure 13.3.1 shows the block diagram of the ΔΣ modulator. A 5th-order CT feedforward loop filter is implemented with 2 programmable notches that suppress the quantization noise at the edge of the signal band. A 1b quantizer is used together with a 1b inherently linear SC feedback DAC.

The loop filter consists of 5 RC integrator stages that use identical OTA circuits. The feedforward coefficients are implemented with resistors that are combined on a virtual-ground node. The virtual-ground node is implemented with the same OTA circuit as used in the integrators. Because of the CT nature of the filter, high alias suppression is guaranteed.

Extensive programmability is introduced in the ADC in order to optimize the performance for each specific bandwidth-clock combination. The sample frequency of the modulator can be programmed from 13MHz to 400MHz and is split into 11 sub-ranges. In order to implement the desired unity-gain frequencies, each sample frequency sub-range requires a separate set of capacitor values for the integrators in the loop filter. Each mode re-uses part of the biggest capacitance that is required for the lowest clock range. In this way, the area overhead for multi-mode operation is minimized. The signal bandwidth of the ADC is programmed via the 2 local feedback coefficients that implement local resonators and realize the notches in the loop filter. Those coefficients are implemented with resistors, and can be set to 11 different values. By re-using the resistor values in each clock-defined mode, only 11 resistor values are required. The combination of these feedback resistors and different integrator capacitors in the loop filter provides the 121 different bandwidth settings that are displayed in Fig. 13.3.2. As indicated in the figure, at low oversampling ratios, the quantization noise is the dominant noise contributor, while at high oversampling ratios the circuit noise is dominant. The reference current of each of the circuits used in the ΔΣ modulator is programmable with 4b resolution. In this way, the minimum required power consumption can be set in each mode depending on bandwidth and noise requirements.

For the feedback DAC, a SC implementation is chosen. The SC DAC minimizes the impact of clock jitter noise [3] in the signal bandwidth caused by out-of-band interferers. The capacitors in the feedback DAC are also programmed for different sample frequencies, as the feedback current is proportional to f_s·C and has to match the input signal current.

A common issue in all high frequency modes is the increased susceptibility to loop delays. The loop delay decreases the phase margin in the loop and might lead to unwanted limit cycles [4] that deteriorate the noise shaping.

The OTA that is used in the integrator stages and in the summing stage is the most challenging circuit from design perspective. The OTA has to achieve a high DC gain, required for all modes, and high bandwidth, required for the high clock frequency modes, with very low thermal and flicker noise levels.

Figure 13.3.3 shows the schematic diagram of the OTA. The OTA uses two stages with parallel inputs: an inner two-stage amplifier realizes the high DC gain and an outer single stage amplifier assures the high frequency operation. The inner stage consists of the input pair M1/M2, current sources M3/M4, output stage M5/M6, and cascode transistors M7/M8. The common-mode voltage at the output of the inner-loop input pair is set by the V_{gs} of the current sources M3/M4 via resistors R1 and R2. The outer-stage input pair realizes a high-frequency bypass path that feeds the input signal directly to the output in order to increase the bandwidth of the OTA. The common-mode voltage of the outer loop is set by current source M11. A common-mode circuit connected to the output of the OTA controls the gate voltage of M11. By using an inner- and outer-loop OTA, a good compromise is found between speed, noise, and DC gain, without a power-consumption penalty.

A block diagram and layout of the prototype chip are shown in Fig. 13.3.7. The IC is fabricated in a 1P 6M 90nm CMOS process. It includes 2 ADCs, a bandgap reference, a digital decimation filter, and a serial interface for programming. The modulator operates from 1.1V to 1.3V with only 2dB SNR variation and uses between 1.44mW and 7mW from the native 1.2V supply.

In Fig. 13.3.2, the measured (crosses) SNR in a number of relevant modes is compared with the calculated (lines) one. The simulated and measured values match within 2dB. The power efficiency is indicated by the FOM given for several characteristic modes.

Figure 13.3.4 shows an inter-modulation measurement of a single ΔΣ modulator. The IM2 is better than 70dB and the IM3 is better than 80dB for all modes.

The programmability in clock frequency is shown in Fig. 13.3.5, where 4 output spectra of the I/Q ΔΣ modulators for different modes that are clocked with different clock frequencies are shown. From the 4 output spectra, an IR of better than 50dB is concluded. A summary of the measured performance is presented in Fig. 13.3.6.

A multi-mode CT DS ADC that achieves a competitive FOM (from 0.2pJ/conv. to 0.8pJ/conv.) over 121 modes has been presented. The modulator is programmable in bandwidth over two decades (0.1MHz to 10MHz), SNR (85dB to 52dB) and power (1.44mW to 7mW). It combines the advantages of low-jitter sensitivity of SC ΔΣ modulators and high anti-alias suppression of CT ΔΣ modulators. This low-power high-resolution multi-mode modulator enables a low-cost, highly integrated receiver and considerably decreases time-to-market.

References:

[1] R. H. M. van Veldhoven, "A Triple-Mode Continuous-Time ΣΔ Modulator with Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2K/UMTS Receiver," *IEEE J. Solid State Circuits*, vol. 38, pp. 2069-2076, Dec., 2003.

[2] J. Arias, P. Kiss, V. Prodanov, et al., "A 32-mW 320-MHz Continuous-Time Complex Delta-Sigma ADC for Multi-Mode Wireless-LAN Receivers," *IEEE J. Solid State Circuits*, pp. 339-351, vol. 41, Feb., 2006.

[3] R.H.M. van Veldhoven, P.A.C.M. Nuijten, P. van Zeijl, "The Effect of Clock Jitter on the Spectral Performance of Sigma Delta Modulators," *Proc. ISCAS*, pp. 2009–2012, May, 2006.

[4] S.F. Ouzounov, H. Hegt, A. van Roermund, "Sigma-Delta Modulators Operating at a Limit Cycle," *Transaction on Circuits and Systems II*, vol. 53, pp. 399–403, May, 2006.

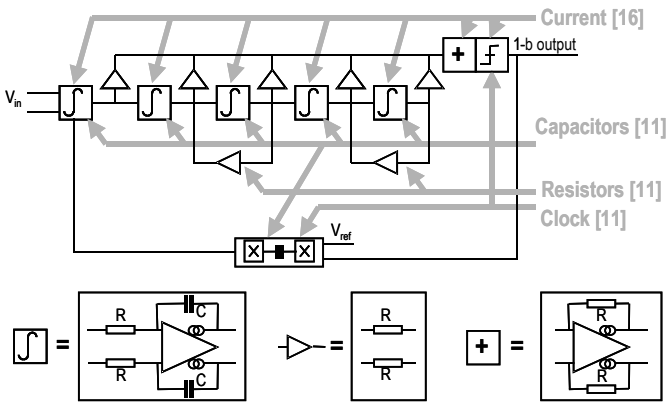

Figure 13.3.1: Programmable 5th-order 1b CT ΔΣ modulator with SC DAC.

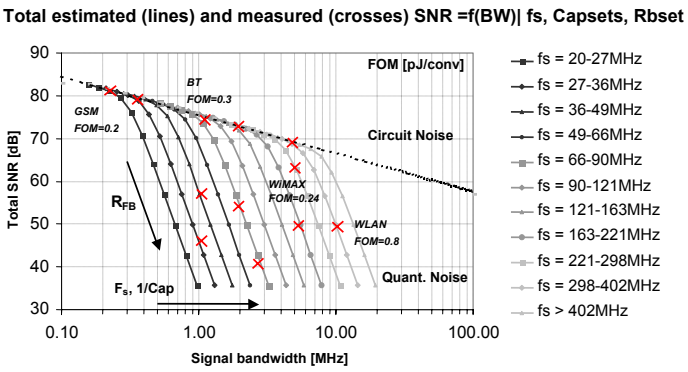

Figure 13.3.2: Multi-mode implementation: calculated (lines) and measured (crosses) performance with FOM.

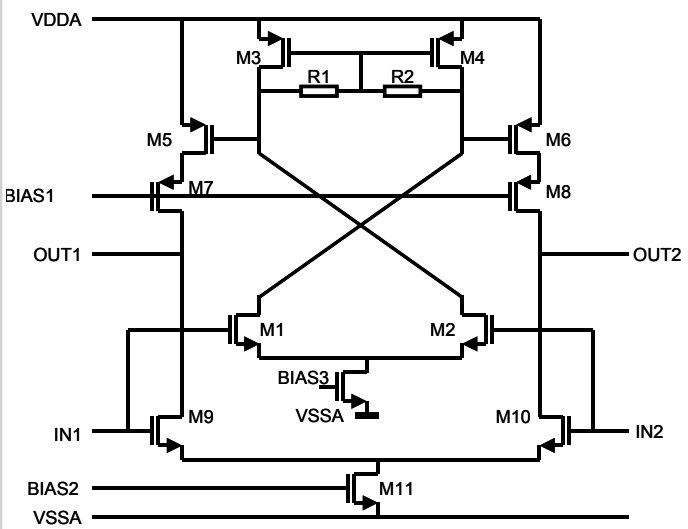

Figure 13.3.3: OTA circuit of integrators and summing stage.

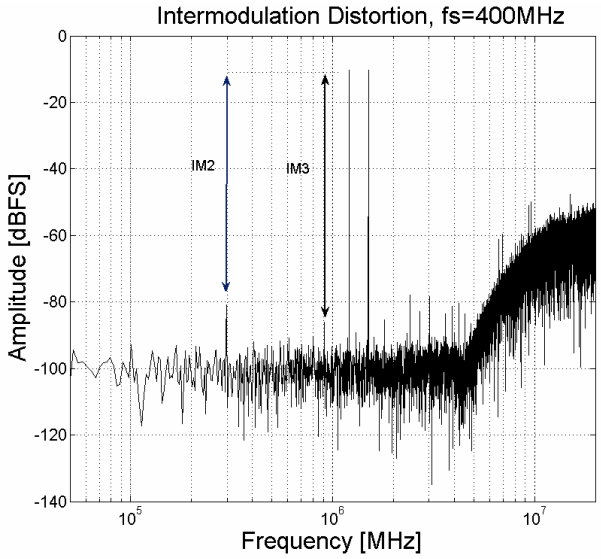

Figure 13.3.4: Measured IM2/IM3.

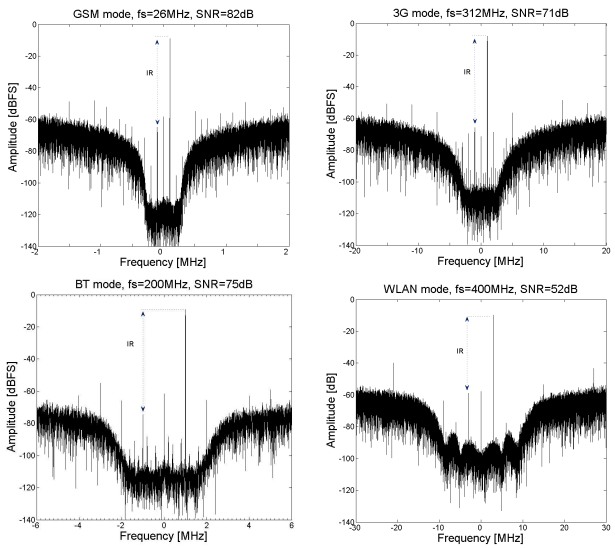

Figure 13.3.5: Measured I/Q spectra and IR for 4 clock settings.

Process	1P 6M standard 90nm			
Supply voltage	1.1V – 1.3V (±3dB DR performance deviation)			
ΔΣ modulator	5th-order CT, feedforward, 1-b with SC DAC			
Input voltage range	0.45V_{rms}, differential			
Modes	121	GSM	BT	WLAN
Sampling rate	13MHz - 400MHz	26MHz	200MHz	400MHz
Signal bandwidth	100kHz - 10MHz	200kHz	1MHz	10MHz
Dynamic range	52dB - 82dB	82dB	75dB	52dB
Intermod. distances	IM2 > 70dB IM3 > 75dB			
Image Rejection	> 50dB			
Power@1.2V, one ΔΣ modulator	1.44mW - 7mW	1.44mW	3.4mW	7mW
FOM	0.2pJ/conv. - 0.8pJ/conv.	0.2pJ/conv.	0.31pJ/conv.	0.8pJ/conv.

Figure 13.3.6: Summary of measured performance.

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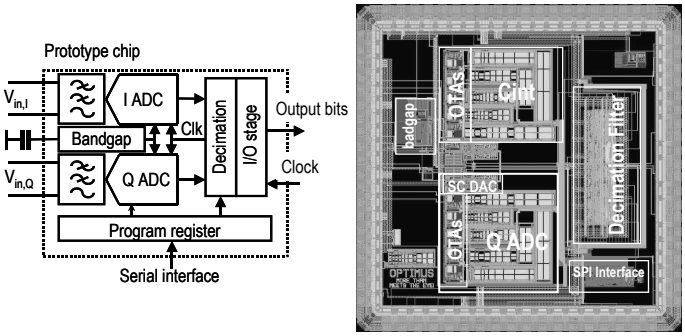

Figure 13.3.7: Block diagram and layout of prototype chip.

